ASP-DAC 2024 - Designers' Forum

Session (2) Heterogeneous Integration and Chiplet Design

Time	23 January, 2023 (Tuesday)
Location	Room 110/111
Organizer	Rino Choi (Inha University, Korea)
Co-Chair	Rino Choi (Inha University, Korea) Jaeduk Han (Hanyang University, Korea)

1. Co-Design Considerations of Heterogeneous Integrated Packaging

Speaker: Gu-Sung Kim (Professor, Kangnam University, Korea)

Abstract:

Modern Semiconductor technology is a position representing competitiveness among countries. Due to the preoccupation of semiconductor front-end technology by a few countries, most of the countries that were left out of ranks are strengthening support for semiconductor back-end technology, such as China, Japan, Southern Asia, and Europe. Unlike the eight major semiconductor processes, it is difficult to understand the flow of the entire technology in the semiconductor back-end process due to its diversity and variability. Heterogeneous Integration is new era technology, integration of separately manufactured into a higher-level assembly that provides functional improvements. The Presenter explains the semiconductor Back-End Process and Technology, from the assembly technology mentioned in the ITRS last version to the Heterogeneous Integration technology in the IEEE EPS HIR, in connection with Moore's Law. In addition, present what is considerable design concepts including electrical, mechanical, and thermal simulations in this area.

2. Don't Close Your Eyes on Temperature: System Level Thermal Perspectives of 3D Stacked Chips

Speaker: Sung Woo Chung (Professor, Korea University, Korea)

Abstract:

With the limited process technology scaling, heterogeneous integration becomes a viable solution to elevate system performance. For heterogeneous integration, 3D stacking is one of the attractive solutions since it leads to small area. However, 3D stacking inevitably causes higher on-chip temperature due to high power density, which negatively affects processing units and DRAM as follows: 1) When on-chip temperature of the processing units such as CPU, GPU, and NPU reaches threshold temperature, DTM(Dynamic Thermal Management) is invoked to reduce power consumption (which eventually sustains on-chip temperature). For DTM, frequency

and (or) voltage is decreased leading to system performance degradation. 2) When on-chip temperature of DRAM (HBM) goes over threshold temperature, DRAM should be refreshed more frequently to safely store data, resulting in refresh energy increase and system performance degradation. In this talk, experimental results on Intel Lakefield (first TSV-based CPU) and AMD 5800X3D (first C2C-based CPU; actually, last level cache is stacked) are presented. Additionally, additional refresh overhead due to high on-chip temperature (mainly dissipated from a processing unit through silicon via) in HBM is presented.

3. Introducing UCIe: The Global Chiplet Interconnect Standard

Speaker: Youngbin Kwon (Engineer, Samsung Electronics, Korea)

Abstract:

As the chiplet business gains momentum in the HPC (High-Performance Computing) market, several chiplet interconnect standards have emerged and vied for global standardization. Throughout this process, two standards, UCIe (Universal Chiplet Interconnect Express) and BoW (Bunch of Wire), have persevered. UCIe, in particular, has garnered significant attention as a potential global standard, primarily due to its robust consortium backing. Additionally, unlike other standards, UCIe offers support for widely used protocols in the HPC field, such as PCIe and CXL. This talk aims to introduce the key characteristics of UCIe, delve into an overview of the UCIe Transceiver Structure, and highlight its major electrical parameters. Furthermore, this talk will briefly touch upon the current development trends of IP vendors within the UCIe ecosystem.

4. Addressing Modeling and Simulation Challenges in Chiplet Interfaces

Speaker: Jaeha Kim (Professor, Seoul National University, Korea)

Abstract:

High-speed die-to-die interfaces are essential in enabling chiplets, the emerging building blocks for heterogeneous integration. Interestingly, many chiplet interface standards including Universal Chiplet Interconnect Express (UCIe) are evolving in ways so that the analog circuits become standardized blocks, and the digital finite-state machines (FSMs) provide complex functionalities. While such architecture can improve design efficiency and portability, it presents new challenges for verifying the overall system functionalities. This talk will use an example of modeling both the analog circuits and digital FSMs of a UCIe physical layer in SystemVerilog and discuss how one can combine the analog and digital approaches to functional verification.